ABSTRACT OF THE DISCLOSURE

A semiconductor wafer fabrication system that includes at least a track system and a scanner system compensates for deviations from nominal periodicity in the scanner system by dynamically introducing time delays when such deviations are detected. Preferably prior art static wait states are also introduced into the wafer recipe to reduce probability of resource conflicts. The resultant semiconductor wafer fabrication system can enjoy enhanced wafer throughput in that synchronization of wafer flow is maintained, despite such deviations.